

**WHAT IS CLAIMED IS:**

1 1. A method for managing latency comprising:  
 2 receiving data from a high-order synchronous transport  
 3 module (STM) and synchronous transport signal (STS) sources  
 4 and low-order tributary unit (TU) and virtual tributary  
 5 (VT) sources;  
 6 providing a provisioning bit for each output associated  
 7 with a memory; and  
 8 adjusting a pointer for the low-order sources based on  
 9 the provisioning bit such that the high-order and low-order  
 10 outputs are synchronized.

1 2. The method of claim 1 further comprising determining an  
 2 adjustment for the pointer based on a predetermined delay.

1 3. The method of claim 1 wherein adjusting the pointer  
 2 includes adjusting the pointer by a predetermined number of  
 3 time slots.

4 4. The method of claim 1 further comprising  
 5 assembling synchronized outputs from the memory.

1 5. The method of claim 1 further comprising  
 2 adjusting the pointer to synchronize the output of the  
 3 high-order and low-order sources, wherein the high-order  
 4 sources incur less delay to pass through the memory than  
 5 low-order sources.

1 6. The method of claim 1 wherein providing a provisioning bit  
 2 includes storing the provisioning bit in a connection  
 3 memory.

1 7. The method of claim 1 wherein adjusting a pointer for the  
2 low-order sources based on the provisioning bit includes  
3 adjusting the pointer when the provisioning bit is set.

1 8. The method of claim 7, further comprising  
2 setting the provisioning bit for low-order sources.

1 9. The method of claim 1 wherein adjusting a pointer for the  
2 low-order sources based on the provisioning bit includes  
3 not adjusting the pointer when the provisioning bit is not  
4 set.

1 10. The method of claim 9 further comprising  
2 setting the provisioning bit for high-order sources.

1 11. A computer program product tangible embodied on a  
2 computer readable medium, for provisioning cross-connects  
3 in network switching environment comprising instructions  
4 for causing a computer to:  
5 receive data from high-order synchronous transport module  
6 (STM) and synchronous transport signal (STS) sources and  
7 low-order tributary unit (TU) and virtual tributary (VT)  
8 sources;  
9 provide a provisioning bit for each output associated  
10 with a memory; and  
11 adjust a pointer for the low-order sources based on the  
12 provisioning bit such that the high-order and low-order  
13 outputs are synchronized.

1 12. The computer program product 11 further comprising  
2 instructions for causing a computer to:

3       determine an adjustment for the pointer based on a  
4       predetermined delay.

1       13.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:  
3       adjust the pointer by a predetermined number of time  
4       slots.

1       14.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:  
3       assemble synchronized outputs from the memory.

1       15.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:  
3       adjust the pointer to synchronize the output of the low-  
4       order and high-order sources, wherein the high-order  
5       sources incur less delay to pass through the memory than  
6       low-order sources.

1       16.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:  
3       store a provisioning bit in a connection memory.

1       17.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:  
3       adjust a pointer for the low-order sources based on the  
4       provisioning bit includes adjusting the pointer when the  
5       provisioning bit is set.

1       18.       The computer program product of claim 11 further  
2       comprising instructions for causing a computer to:

3        adjust a pointer for the low-order sources based on the  
4        provisioning bit includes not adjusting the pointer when  
5        the provisioning bit is not set.

1        19.        An apparatus including:

2            a memory for storing a provisioning bit for each output  
3            associated with a memory;

4            a first circuit configured to receive data from high-  
5            order synchronous transport module (STM) and synchronous  
6            transport signal (STS) sources and low-order tributary unit  
7            (TU) and virtual tributary (VT) sources;

8            a second circuit configured to adjust a pointer for the  
9            low-order sources based on the provisioning bit such that  
10          the high-order and low-order outputs are synchronized.

1        20.        The apparatus of claim 19 wherein the second circuit  
2        is configured to adjust the pointer by a predetermined  
3        number of time slots.

1        21.        The apparatus of claim 19 wherein the second circuit  
2        is configured to adjust the pointer to synchronize the  
3        output of the high-order and low-order sources, wherein the  
4        high-order sources incur less delay to pass through the  
5        memory than low-order sources.

1        22.        The apparatus of claim 19 wherein the memory is a  
2        connection memory.